THIN FILM TRANSISTOR ARRAY PANEL

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority from and the benefit of Korean Patent Application No. 10-2015-0082716, filed on Jun. 11, 2015, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND

Field

Exemplary embodiments relate to a thin-film transistor array panel, and more particularly, to a thin-film transistor array panel including self-assembled monolayers.

Discussion of the Background

A thin-film transistor (TFT) may be used in various electronic devices such as a flat panel display or the like. A TFT may be used as a switching element or a driving element in a flat panel display, such as a liquid crystal display (LCD), an organic light emitting diode (OLED) display, an electrophoretic display, or the like.

A TFT may include a gate electrode connected to a gate line that transmits a scanning signal, a source electrode connected to a data line that transmits a signal to be applied to a pixel electrode, a drain electrode that faces the source electrode, and a semiconductor electrically connected to the source electrode and the drain electrode.

A semiconductor may be formed of amorphous silicon, polysilicon, or an oxide semiconductor. A TFT may maintain a predetermined threshold voltage, however the threshold voltage may be non-uniform or may be shifted depending on the type of the semiconductor. As such, when the threshold voltage is non-uniform or shifted, a separate compensation circuit may be added.

The above information disclosed in this Background section is only for enhancement of understanding of the background of the inventive concept, and, therefore, it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

SUMMARY

Exemplary embodiments of the present invention provides a thin-film transistor array panel that may control a threshold voltage without a separate compensation circuit.

Additional aspects will be set forth in the detailed description which follows, and, in part, will be apparent from the disclosure, or may be learned by practice of the inventive concept.

An exemplary embodiment discloses a thin-film transistor array panel including a substrate, a first gate electrode disposed on the substrate, a first self-assembled monolayer disposed on the first gate electrode, a gate insulating layer disposed on the first self-assembled monolayer, a semiconductor disposed on the gate insulating layer, a drain electrode overlapping the semiconductor, the drain electrode being separated from and facing a source electrode with respect to the semiconductor, a first interlayer insulating layer disposed on the source electrode and the drain electrode, a second self-assembled monolayer disposed on the first interlayer insulating layer, a second gate electrode disposed on the second self-assembled monolayer, a second interlayer insulating layer disposed on the second gate electrode, and a pixel electrode disposed on the second interlayer insulating layer and connected to the drain electrode.

An exemplary embodiment also discloses a method of forming a thin-film transistor array panel including forming a first gate electrode on a substrate, forming a first self-assembled monolayer on the first gate electrode, forming a gate insulating layer on the first self-assembled monolayer, forming a semiconductor on the gate insulating layer, forming a drain electrode overlapping the semiconductor, the drain electrode being separated from and facing a source electrode with respect to the semiconductor, forming a first interlayer insulating layer on the source electrode and the drain electrode, forming a second self-assembled monolayer on the first interlayer insulating layer, forming a second gate electrode on the second self-assembled monolayer, forming a second interlayer insulating layer on the second gate electrode, and forming a pixel electrode on the second interlayer insulating layer and connected to the drain electrode.

According to exemplary embodiments, a thin-film transistor array panel may be configured to control a threshold voltage without a separate compensation circuit.

The foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the claimed subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the inventive concept, and are incorporated in and constitute a part of this specification, illustrate exemplary embodiments of the inventive concept, and, together with the description, serve to explain principles of the inventive concept.

FIG. **1** is a layout view of a thin film-transistor array panel according to exemplary embodiments.

FIG. **2** is a cross-sectional view taken along lines II-IF and II'-II" of FIG. **1**.

FIG. **3** is a layout view of a thin-film transistor array panel according to exemplary embodiments.

FIG. **4** is a cross-sectional view taken along lines IV-IV' and IV'-IV" of FIG. **3**.

FIG. **5** is a layout view of a next step of FIG. **3**.

FIG. **6** is a cross-sectional view taken along lines VI-VI' and VI'-VI" of FIG. **5**.

FIG. **7** is a layout view of a next step of FIG. **5**.

FIG. **8** is a cross-sectional view taken along lines VIII-VIII' and VIII'-VIII" of FIG. **7**.

FIG. **9** is a layout view of a next step of FIG. **7**.

FIG. **10** is a cross-sectional view taken along lines X-X' and X'-X" of FIG. **9**.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of various exemplary embodiments. It is apparent, however, that various exemplary embodiments may be practiced without these specific details or with one or more equivalent arrangements. In other instances, well-known structures and devices are shown in block diagram form in order to avoid unnecessarily obscuring various exemplary embodiments.